

Notice of Allowability	Application No.	Applicant(s)	
	09/930,956	KOYAMA ET AL.	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCE and IDS filed on 7/14/2006.
2. ☒ The allowed claim(s) is/are 1-53 and 62.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>7/14/2006</u> 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____. |
|---|--|

Allowable Subject Matter

1. Claims 1-53 and 62 allowed.
2. The following is an examiner's statement of reasons for allowance:

The claimed invention is directed to a liquid crystal display device with low power consumption by using a driver circuit and a pixel that have novel circuit structures. In a liquid crystal display device using n (n is a natural number and satisfies $n \geq 2$) bit digital video signals to display an image, $n \times m$ (m is a natural number) memory circuits and $n \times k$ (k is a natural number) non-volatile memory circuits are provided in each pixel, thereby giving the device a function of storing m frames of digital video signals in the memory circuits and a function of storing k frames of digital video signals in the non-volatile memory circuits.

Independent claim 1 identifies the uniquely distinct features "a plurality of read transistors, wherein each of the plurality of read transistors is electrically connected to a corresponding one of the plurality of first switches, and to a corresponding one of the plurality of second switches; a plurality of write transistors, wherein each of the plurality of write transistors is electrically connected to a corresponding one of the plurality of third switches, and to a corresponding one of the plurality of fourth switches."

Independent claim 12 identifies the uniquely distinct features " n read transistors, wherein each of the n read transistors is electrically connected to a corresponding one of the n first switches, and to a corresponding one of the n second switches; n write transistors, wherein each of the n write transistors is electrically connected to a

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corresponding one of the n third switches, and to a corresponding one of the n fourth switches.”

Independent claim 23 identifies the uniquely distinct features “where each gate electrode of the n writing transistors is electrically connected to one of the n writing gate signal lines, with no two gate electrodes sharing the same writing gate signal line ... wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the $n \times k$ non-volatile memory circuits through one of n units of the $2n$ non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode.”

Independent claim 36 identifies the uniquely distinct features “wherein each input electrode of the n writing transistors is electrically connected to one of the n source signal lines, with no two input electrodes sharing the same source signal line, ... wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the $n \times k$ non-volatile memory circuits through one of n units out of the $2n$ non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode.”

Independent claim 50 identifies the uniquely distinct features “wherein the following (a) through (e) are available and one of the following (a) through (e) is selected and conducted in pixels in the row of the selected gate signal line out of the plural pixels:

(a) the n bit digital video signals inputted from the source signal line are written in memory circuits;

(b) the n bit digital video signals stored in the memory circuits are read;

(c) the n bit digital video signals inputted from the source signal line or the n bit digital video signals stored in the memory circuits are written in non-volatile memory circuits;

(d) the n bit digital video signals stored in the non-volatile memory circuits are read; and

(e) the n bit digital video signals stored in the non-volatile memory circuits are written in the memory circuits.”

Independent claim 62 identifies the uniquely distinct features “a write transistor electrically connected to the first switch and to the second switch; and a read transistor electrically connected to the third switch and to the fourth switch.”

The closest prior art, Okumura et al. (US 5,945,972, hereinafter Okumura), teaches a liquid crystal display sub-pixel having two memory elements with respective input and output transfer gates. The input side of each input transfer gate is connected directly to a data line and the output side of each output transfer gate is connected directly to a liquid crystal cell. There are no read transistor and write transistor connected to each set of the n sets of memories. Thus, Okumura fails to anticipate or render obvious the above claim features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

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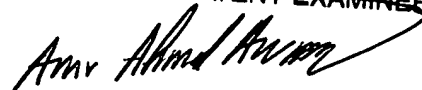
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Sheng
September 25, 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

A handwritten signature in black ink, appearing to read "Amr A. Awad", written over the printed name and title.